Supercomputer I:

1.) The routing table network of the device through fiber optics makes the difference of that of the flow of information for that of the binary gate array configuration routing the differences of signals and their multiplicative geometry algebraically for that of the primitive operations of strict logical relation of gate structures through that of the order of operations and a mixed interpretative validity of machine states by blocking, freedom, and constraint to that of resilient control flow graphs in the active pre-processor.

2.) This routing table is configured in hardware and negotiates the binary flow control structure to enable the flow of information into a halting table at light speed for that a gaussian or normalized distribution setup of free circular embedding and extensibility of control mechanism known by various means as that which is light enable and light disable through the flow of light by extensibility of the machine state from preliminary blocks of information in two dimensions with the third dimension of depth and temporally existent evolution with that of dynamic reprogrammability with control structure elements via control signals of two frequencies.

3.) The persistence window as a design consideration is preliminarily bigger on the side of the touchscreen stylus adaptation with that of the device stack for that of the processing stack for that of the smaller effective area; and yet equivalent in timing for that geometric coextensibility via equivalent areal difference of individual pallets; for that of what is an effective window of operation in time by which persistence of signal structures may be represented equivalently on one touch screen and device stack with the given consideration of persistence through that of dynamic signal generation and scanning; for that of what are effectively differential commands and signals when exclusively the differences in frequencies do not overlap; the freedom of which is afforded in order for that of by that which is the free flow of the binary bit digital control structure graph due to order of operations; for free information processing for a universal program execution table in hardware at the effective speed of the quotient of the hardware to software.

4.) The interfacial input and output of the signal driver of one nature and the input of a differential variety and output of additional differential variety for that of the frequency generator and that of the analog to digital converter for top and bottom are selectively bridged into the structure for that of frequency and signal insertion by which the structure processes dynamically a multiplicity of selective frequencies; with the strict input and output from that of the frequency generator and the analog to digital converter a selector for that of parallel signal pathway without alternation of signal fidelity or data information content as a signal synthesizer and analyzer with that of selectivity and sensing by which the processing may be monitored; offering a method to dynamically monitor information processing through the system; and operating in coparallel with that of differential methods of data recovery; therefore the signal pathways are configured with the design principle of seamlessness of exclusive and nonexclusive (inclusive) considerations for that of what you see is what you get stylus input with frequency selectivity and that of program interactivity.